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Distribution of Timing: Basics principle and Sync over the Physical Layer

WSTS Tutorial – 09 May 2022

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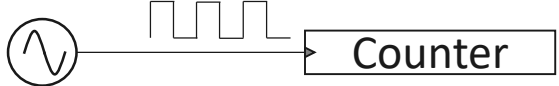
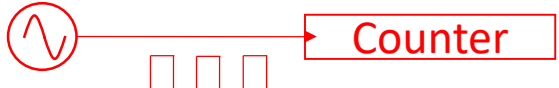
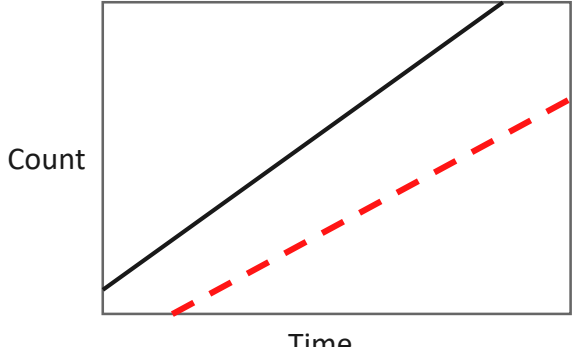
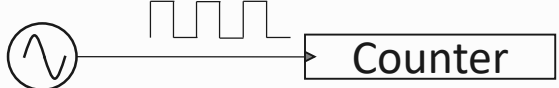
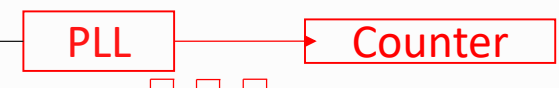
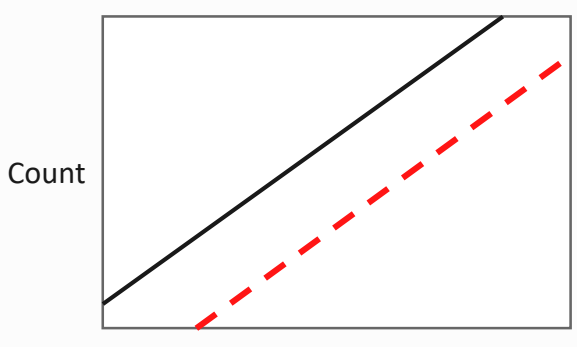
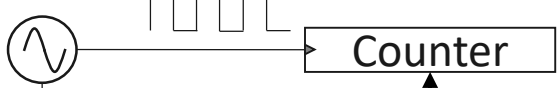
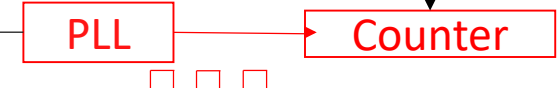
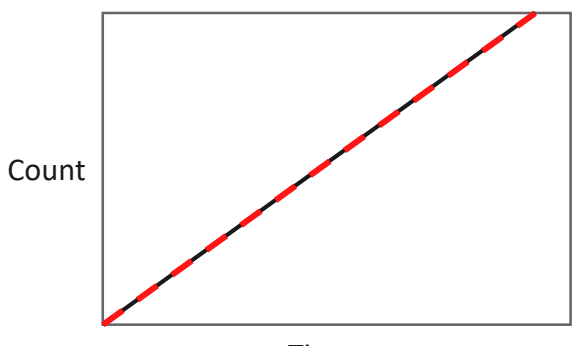


Credits:

- Figures in slides 5, 6, 9, 15 taken from book «Synchronous Ethernet and IEEE 1588 in Telecoms: Next Generation Synchronization Networks» (Wiley, 2013, ISBN: 978-1-848-21443-9)

1. General

Time vs Frequency

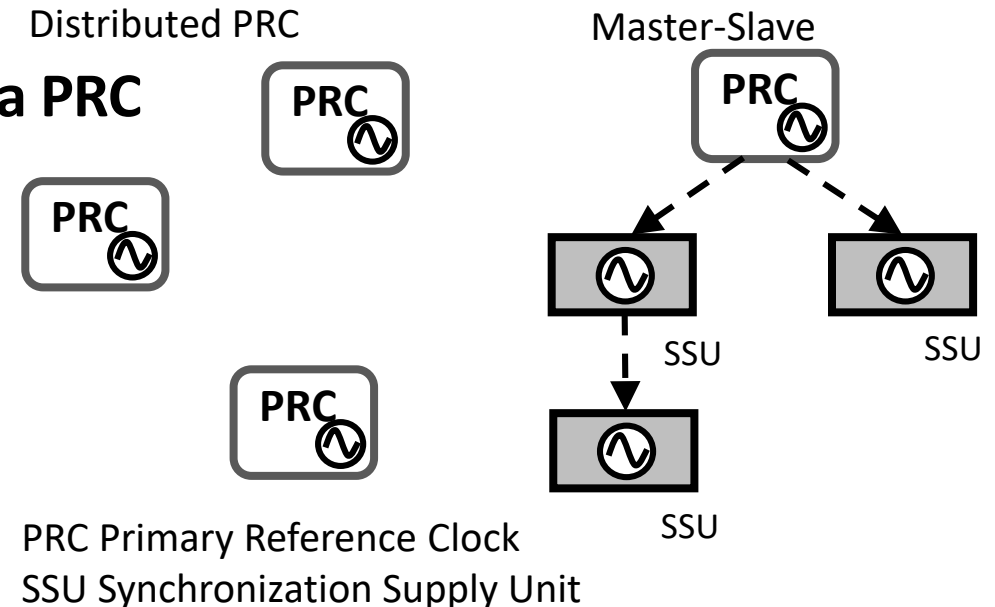
<p>125MHz + x PPM</p>  <p>Counter</p> <p>125MHz + y PPM</p>  <p>Counter</p>	 <p>Count</p> <p>Time</p>	<p>Not Synchronized</p>
<p>125MHz + x PPM</p>  <p>Counter</p> <p>125MHz + x PPM</p>  <p>PLL</p> <p>Counter</p>	 <p>Count</p> <p>Time</p>	<p>Frequency Synchronized (Syntonized)</p>
<p>125MHz + x PPM</p>  <p>Counter</p> <p>125MHz + x PPM</p>  <p>PLL</p> <p>Counter</p> <p>Clear (1PPS)</p> <p>1PPS = 1 Pulse Per Second</p>	 <p>Count</p> <p>Time</p>	<p>Time/Phase Synchronized</p>

Master-Slave vs. Plesiochronous

- Original focus in Telecom is **Frequency synchronization**. Basic concepts defined in ITU-T G.810:
 - **plesiochronous mode** : *A mode where the essential characteristic of time scales or signals such that their corresponding significant instants occur at nominally the same rate, any variation in rate being constrained within specified limits*
 - **master slave mode** : *A mode where a designated master clock is used as a frequency standard which is disseminated to all other clocks which are slaved to the master clock*
 - **mutually synchronized mode** : *A mode where all clocks exert a degree of control on each other*

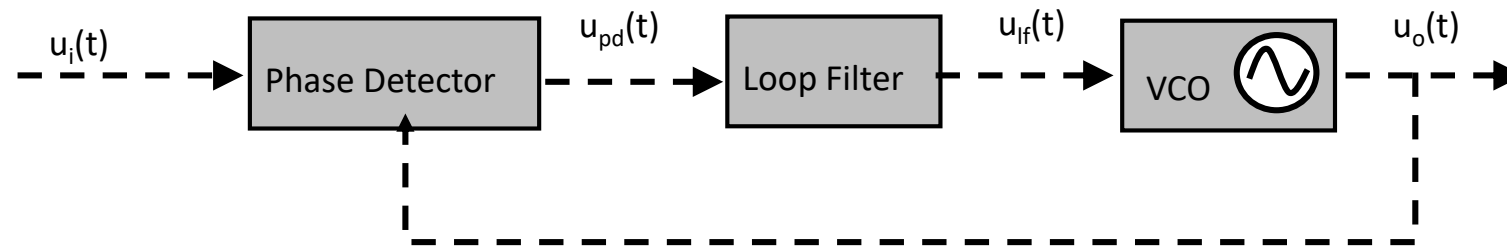
- **Telecom networks were originally synchronized to a PRC**

- PRC were originally based on Cesium technology
- Timing Distribution based on Centralized architectures (based on synchronized mode)
- Increased use of GNSS-based sync leading to a mix of «Distributed PRC» and «synchronized mode»
- Renewed interest on Mutually Synchronized mode in the time sync domain



Basic Technologies: GNSS, Atomic clocks, PLL

- Phase locked loops (PLLs) can be used to form a synchronization chain from a timing source to a timing receiver to deliver time to an end application
- Origin of time in the network :
 - GNSS Receivers
 - Atomic Clocks (Cesium for frequency accuracy better than 10^{-11})



$u_i(t)$ input reference timing signal
 $u_o(t)$ output reference timing signal
 $u_{pd}(t)$ loop filter output signal
 $u_{lf}(t)$ phase detector output signal

Timing Protocols

—NTP, Network Time Protocol defined by IETF

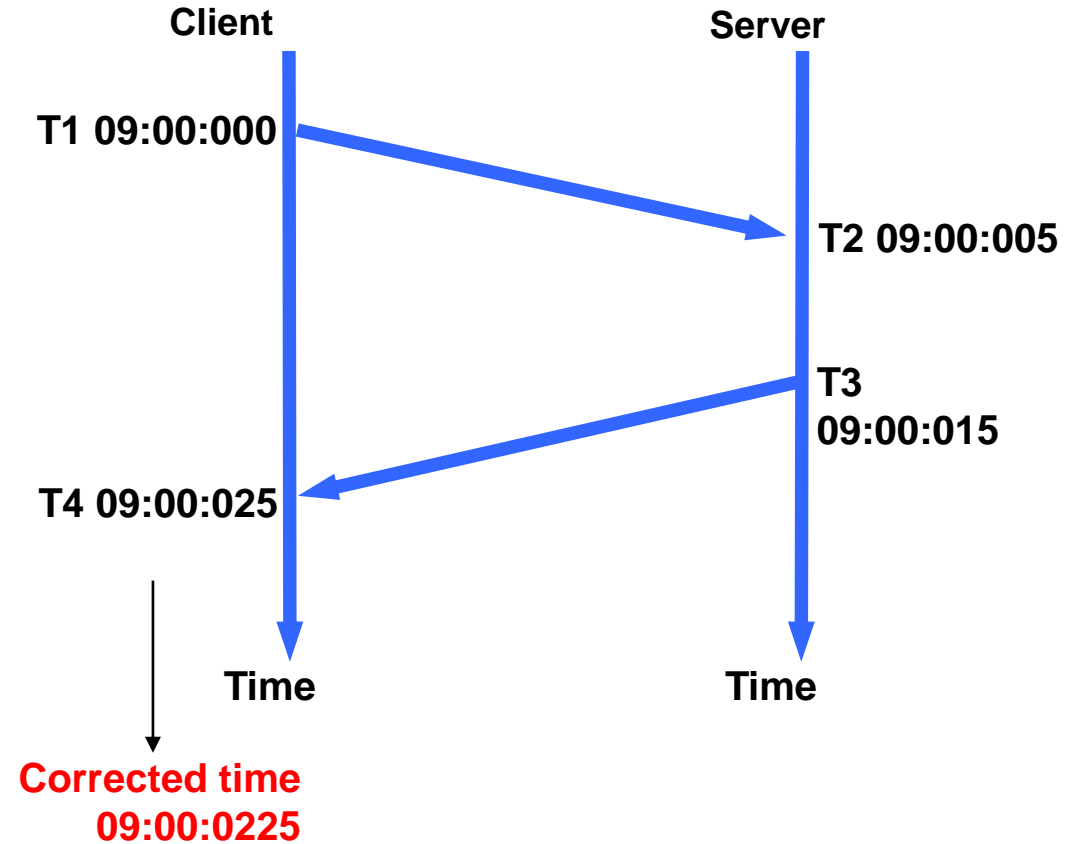
- protocol for clock synchronization between computer systems over packet-switched networks
- RFC 1305 (NTP version 3) 1992
- Latest version v4
 - RFC 5905: Network Time Protocol Version 4: Protocol and Algorithms Specification
 - RFC 5906: Network Time Protocol Version 4: Autokey Specification
 - RFC 5907: Definitions of Managed Objects for Network Time Protocol Version 4 (NTPv4)
 - RFC 5908: Network Time Protocol (NTP) Server Option for DHCPv6

—PTP, Precision Timing Protocol, defined by IEEE 1588

- V1 (2002)
- V2 (2008)
- V2.1 (2019)

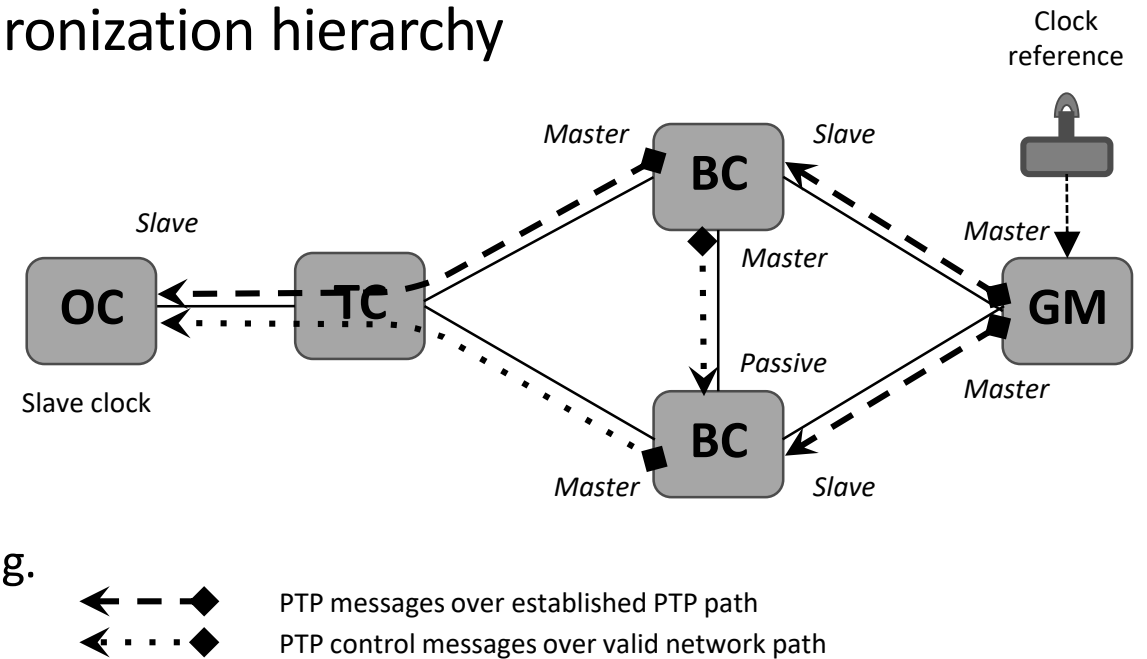
How NTP Works

- T1 Originate Timestamp
 - Time request sent by client
- T2 Receive Timestamp
 - Time request received by server
- T3 Transmit Timestamp
 - Time reply sent by server
- T4 Destination Timestamp
 - Time reply received by client
- Round Trip Delay = $(T4 - T1) - (T3 - T2)$
 - Round Trip Delay = $25 - 10 = 15$
- Clock Offset = $[(T2 - T1) - (T4 - T3)] / 2$
 - Clock Offset = $[5 - 10] / 2 = -2.5$
(Clients actual time when reply received was therefore 09:00:0225)
- Key Assumptions:
 - **One way delay is half Round Trip (symmetry!)**
 - Drift of client and server clocks are small and close to same value
 - Time is traceable



IEEE 1588-2008/2019

- The Grandmaster “reference clock” sends a series of time-stamped messages to slaves.
- Slaves process timestamps and synchronize to the Grandmaster.
- Frequency can be recovered from an accurate time of day reference (but physical layer can also be used)
- Best Master Clock Algorithm to define the synchronization hierarchy
- Accuracy is possible by means of:
 - Proper packet rate (up to 128 per second)
 - Hardware time-stamping (eliminate software processing delays)
 - Timing support in the network (e.g. transparent clocks, boundary clocks)
- New features in 2019:
 - Addition of special ports to allow some technologies (e.g. WiFi and EPON) to use their inherent timing support
 - New optional features (e.g. cumulative rate ratio, performance monitoring)
 - High accuracy profile
 - Security options

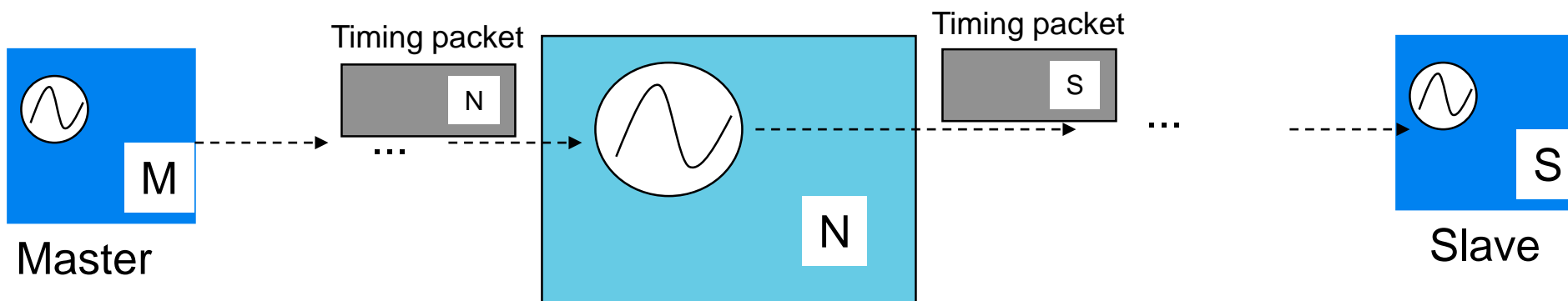


P1588g – Amendment to IEEE 1588 for inclusive terminology

- Amendment Title: Master-slave optional alternative terminology
 - Scope – “This amendment adds an optional alternative suitable and inclusive terminology to the terms: “master” and “slave”, but it does not replace the terms “master” and “slave”.”
 - timeTransmitter and timeReceiver were selected as an alternative nomenclature for master and slave, and it has been used as a basis for the draft amendment
 - SA ballot pool is being formed, it closes on May 13
 - SA ballot will start soon after the SA ballot pool is formed.
- IEEE Std 802.1AS has an amendment to replace offensive words in the standard, and it will be based on P1588g
- Master and Slave are still used in this presentation

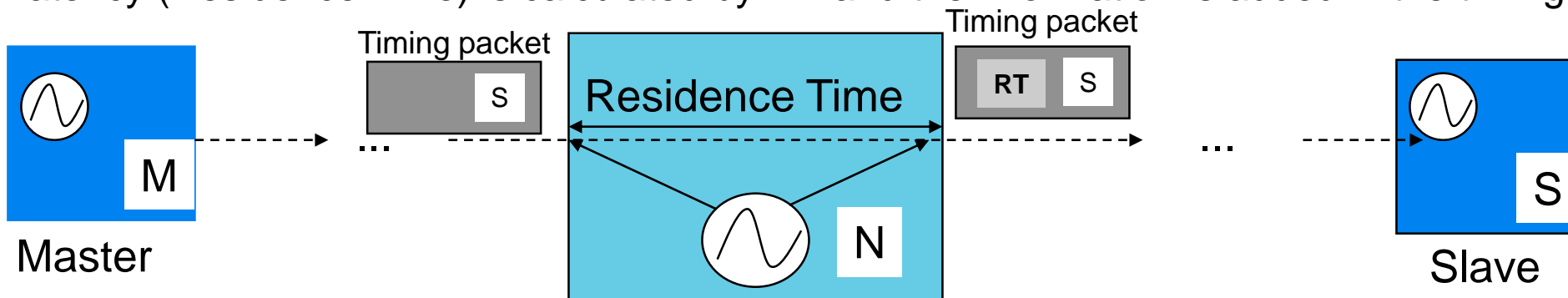
Timing Support

Timing packets are terminated and regenerated by Node N



e.g. **IEEE1588 Boundary Clock**, NTP Stratum Clock

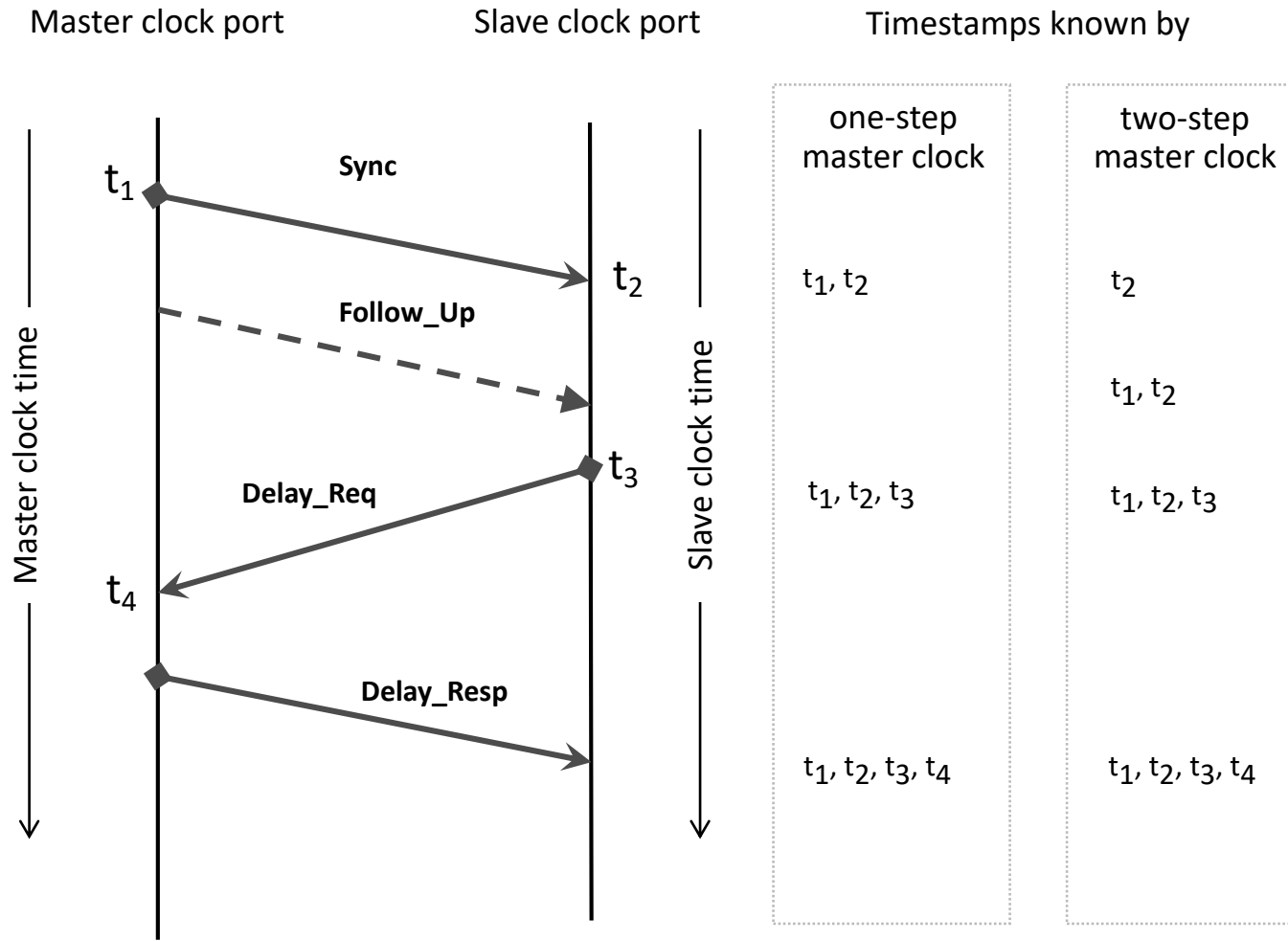
Latency (Residence Time) is calculated by NE and the information is added in the timing packet



e.g. **IEEE1588 Transparent Clock**

To remove (reduce) «Time Error» components internal to the nodes

PTP Time Transfer Technique



Offset:

(slave clock error and one-way path delay)

$$\text{Offset}_{\text{SYNC}} = t_2 - t_1$$

$$\text{Offset}_{\text{DELAY_REQ}} = t_4 - t_3$$

We assume path symmetry, therefore

$$\text{Mean Path Delay} = [(t_2 - t_1) + (t_4 - t_3)] \div 2$$

$$\text{Slave Clock offset} = [(t_2 - t_1) - (t_4 - t_3)] \div 2$$

Notes:

1. One-way delay cannot be calculated exactly, but there is a bounded error.
2. The protocol transfers TAI (Atomic Time).
UTC time is TAI + leap second offset from the *announce* message.

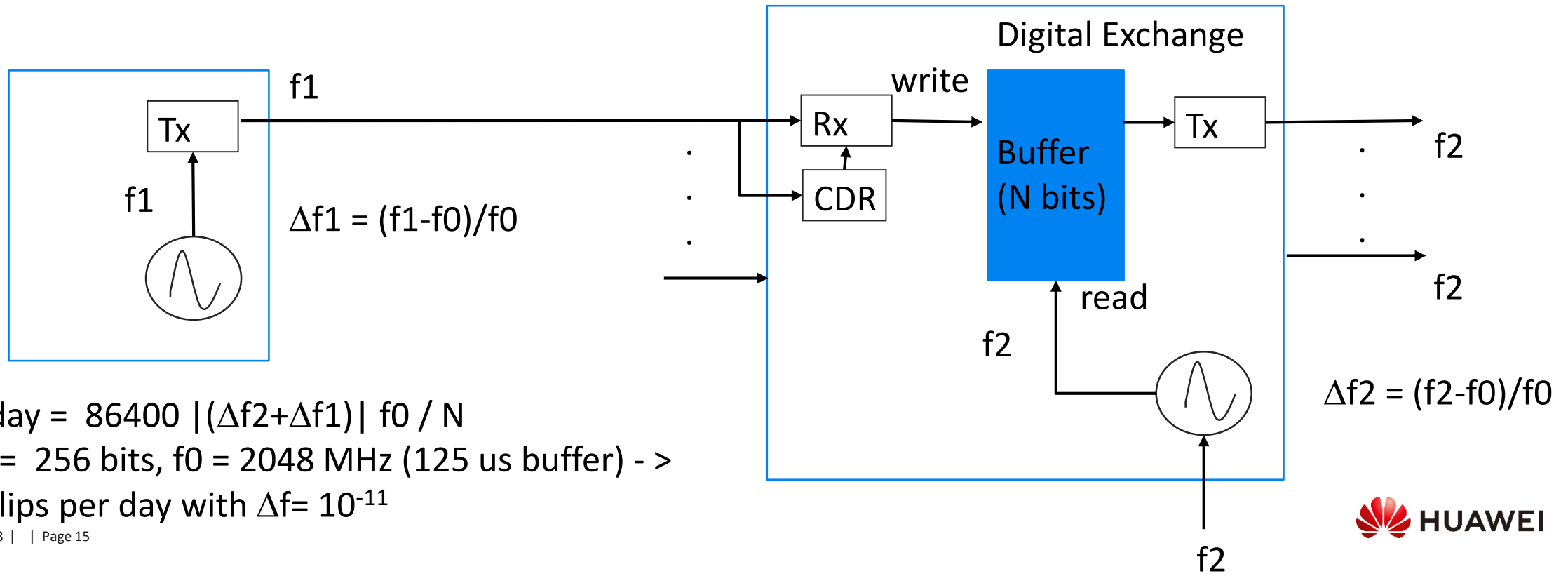
The concept of Profile

- A **profile** is a subset of required **options**, prohibited options, and the ranges and defaults of configurable attributes
- e.g. for Telecom: Update rate, unicast/multicast, etc.
- PTP profiles are created to allow organizations to specify selections of attribute values and optional features of PTP that, when using the same transport protocol, **inter-works** and achieve a **performance** that meets the requirements of a particular application
- Telecom Profiles: G.8265.1, G.8275.1, G.8275.2
- Other (non-Telecom) profiles:
 - IEEE C37.238 (Standard Profile for Use of IEEE 1588 Precision Time Protocol in Power System Applications,)
 - IEEE 802.1AS (Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks)

2. Frequency sync over the Physical layer

Introduction

- Frequency distribution required originally in PDH / SDH-based networks
 - To control the Slip rate (in circuit-switched networks) and control of jitter/wander in SDH networks
 - Timing carried by the bit rate of the traffic signal (typically extracted by the frame alignment word in a TDM frame)
- Slip: «The repetition or deletion of a block of bits in a synchronous or plesiochronous bit stream due to a discrepancy in the read and write rates at a buffer.» (G.810)



$$\text{Slips/day} = 86400 |(\Delta f_2 + \Delta f_1)| f_0 / N$$

Ex.: $N = 256$ bits, $f_0 = 2048$ MHz (125 us buffer) - >

1/72 slips per day with $\Delta f = 10^{-11}$

SyncE: Introduction

- Several applications requiring accurate frequency are reached by Ethernet
 - Since the very start of timing over packet network activities, it was proposed to use a synchronous Ethernet physical layer
 - Not in contradiction with IEEE (10-11 within the +/-100 ppm - 20 ppm)
 - Only in full duplex mode (continuous signal required)
- Based on SDH specification (for interoperability and simplifying the standardization task)
 - Synchronous Ethernet equipment equipped with a synchronous Ethernet Equipment Clock – EEC (G.8262). Synchronous Ethernet interfaces extract the received clock and pass it to the system clock.
 - Synchronization Status Message as per G.8264
 - Enhanced SyncE recently approved (G.8262.1)
 - Recently generalized as physical layer based clock (SEC, Synchronous Equipment Clock)
- It does not transport Time
 - but it was proposed
- All nodes must support SyncE: sync chain as per G.803
 - Cannot be transported transparently across network boundaries

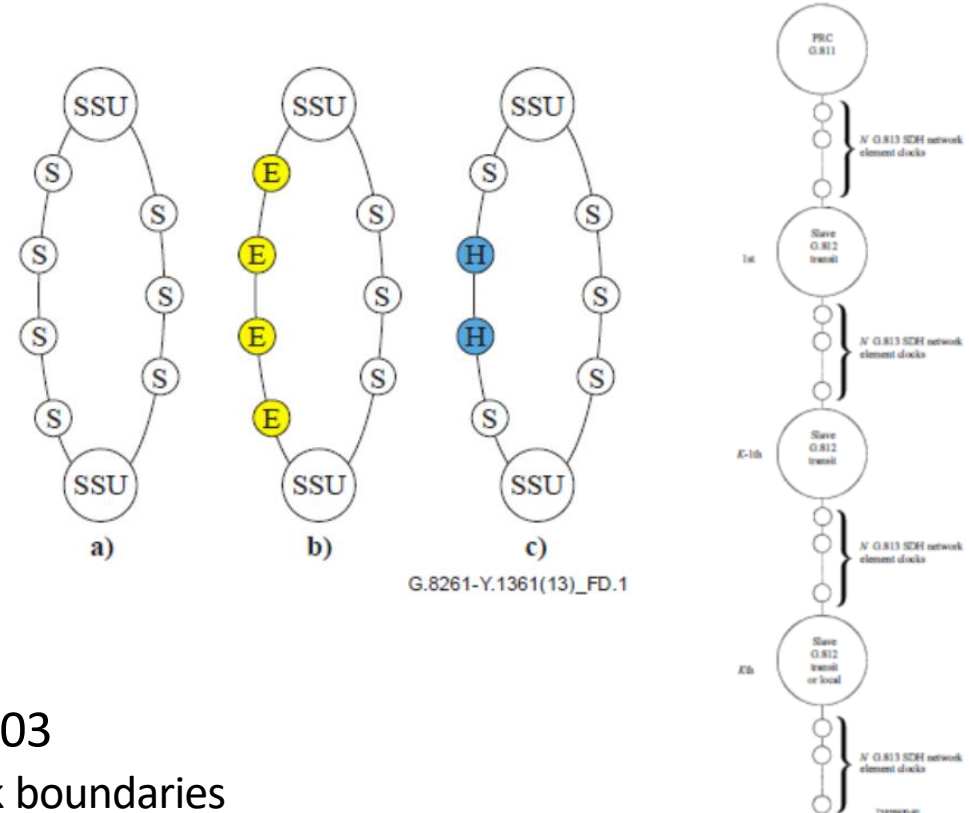


Figure 8-5/G.803 – Synchronization network reference chain

—

- Two types of protocol message types are defined
 - "heart-beat" message (once per second)
 - Event message generated immediately
- SSM QL value is considered failed if no SSM messages are received after a five second period



Ethernet synchronization messaging channel (ESMC) Format

— ESMC PDU with QL TLV always sent as the first TLV in the Data and padding field

Octet number	Size/bits	Field
1-6	6 octets	Destination Address = 01-80-C2-00-00-02 (hex)
7-12	6 octets	Source Address
13-14	2 octets	Slow Protocol Ethertype = 88-09 (hex)
15	1 octet	Slow Protocol Subtype = 0A (hex)
16-18	3 octets	ITU-OUI = 00-19-A7 (hex)
19-20	2 octets	ITU Subtype
21	bits 7:4 (Note 1)	Version
	bit 3	Event flag
	bits 2:0 (Note 2)	Reserved
22-24	3 octets	Reserved
25-1532	36-1490 octets	Data and padding (See point j)
Last 4	4 octets	FCS

Octet number	Size/bits	Field
1	8 bits	Type: 0x01
2-3	16 bits	Length: 00-04
4	bits 7:4 (Note)	0x0 (unused)
	bits 3:0	SSM code

NOTE – Bit 7 of octet 4 is the most significant bit. The least significant nibble, bit 3 to bit 0 (bits 3:0) contains the four-bit SSM code.

NOTE 1 – Bit 7 is the most significant bit of octet 21. Bit 7 to bit 4 (bits 7:4) represent the four number for the ESMC.

NOTE 2 – The three LSBs (bits 2:0) are reserved.

- Recently extended to carry new clock types (and inform on PRTC traceability)
- Extended QL TLV
- Use of Padding bits also recently revised (set to all zero and ignored by receivers)

Extended QL TLV

Octet number	Size/bits	Field
1	8 bits	Type: 0x02
2-3	16 bits	Length: 0x0014
4	8 bits	Enhanced SSM code (see Table 11-6)
5-12	64 bits	SyncE clockIdentity of the originator of the extended QL TLV, Note1,
13	8 bits	Flag; Note2
14	8 bits	Number of cascaded eEECs from the nearest SSU/PRC/ePRC
15	8 bits	Number of cascaded EECs from the nearest SSU/PRC/ePRC
16-20	40 bits	Reserved for future use

SyncE clockIdentity follows the IEEE 1588 rules

Clock	Quality level	Enhanced SSM code
EEC1	QL-EEC1	0xFF
EEC2	QL-EEC2	0xFF
Other clock types contained in [ITU-T G.781] Note 1	QL message (refer to the QL TLV) Note 1	0xFF
PRTC	QL-PRTC	0x20
ePRTC	QL-ePRTC	0x21
eEEC	QL-eEEC	0x22
ePRC	QL-ePRC	0x23

Note: ePRC SSM code (0x23) added in 2018

Note 1: Tables 11-8 and 11-9 illustrate the full set of clock types from [ITU-T G.781]

Thank you!

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